PATENT CLAIMS

1. An arrangement in a communication system including a TDM bus, a number of transmitters and receivers connected to said bus, at least one synchronisation master developing frame synchronisation signals, a clock oscillator, and a timeslot counter in each transmitter/receiver, wherein:

said clock generator is a stable free-running clock generator,

the frequency of said clock generator is selected to give a number of periods within a frame that is always at least one more than the number of timeslots required, the period(s) exceeding this number constituting a dummy period,

each timeslot counter is adapted to identify the dummy period,

the frame synchronisation signals are synchronised to the free-running clock.

2. An arrangement as claimed in claim 1, wherein the dummy period is identified by introducing a carry bit which is set each time the counter(s) exceeds said number.

3. An arrangement as claimed in claim 2, in a system including several synchronisation masters, wherein a switch over to another synchronisation master takes place during the dummy period if the active synchronisation master fail.

4. A method for synchronising a Frame Synchronisation signal (FS) and a data clock signal (CLK) in a TDM-bus system, said system including a number of transmitters and receivers connected to said bus, at least one synchronisation master developing the frame synchronisation signal, a clock oscillator supplying the data clock signal, and a timeslot counter in each transmitter/receiver,
wherein the method includes the following steps:
to develop the FS signal from an external communication signal,
to produce the CLK signal from a free running clock oscillator independent of the FS signal,
to select the frequency of said clock signal (CLK) so that the number of periods within a frame is always at least one more than the number of timeslots required, said period(s) exceeding this number constituting a dummy period,
to synchronise the FS signal to the CLK signal, and supply this synchronised Frame Synchronising signal (FS-S) to the TDM-bus.

5. A method as claimed in claim 4,
wherein a carry bit is introduced in said timeslot counters to identify said dummy period, said carry bit being set each time the counter(s) exceeds the required number of timeslots on the TDM bus.

6. A method as claimed in claim 5,
wherein the system will switch over to another synchronisation master during said dummy period if a synchronisation master fail.